Express Mail Label No. EL 394 376 670 US 05-26-00 A

# UTILITY PATENT APPLICATION TRANSMITTAL
## (Large Entity)

*(Only for new nonprovisional applications under 37 CFR 1.53(b))*

Docket No.
11675.114.1

Total Pages in this Submission
23

**TO THE ASSISTANT COMMISSIONER FOR PATENTS**
**Box Patent Application**
**Washington, D.C. 20231**

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

**GATE STACK STRUCTURE**

and invented by:

**Kei-Yu Ko**

**If a CONTINUATION APPLICATION,** *check appropriate box and supply the requisite information:*

☐ **Continuation** ☒ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: **08/846,671**

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Enclosed are:

**Application Elements**

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having **23** pages and including the following:
   a. ☒ Descriptive Title of the Invention
   b. ☒ Cross References to Related Applications *(if applicable)*
   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   d. ☐ Reference to Microfiche Appendix *(if applicable)*
   e. ☒ Background of the Invention
   f. ☒ Brief Summary of the Invention
   g. ☒ Brief Description of the Drawings *(if drawings filed)*
   h. ☒ Detailed Description
   i. ☒ Claim(s) as Classified Below
   j. ☒ Abstract of the Disclosure

# UTILITY PATENT APPLICATION TRANSMITTAL
## (Large Entity)

*(Only for new nonprovisional applications under 37 CFR 1.53(b))*

| Docket No. |
|---|
| 11675.114.1 |
| Total Pages in this Submission |
| 23 |

**Application Elements (Continued)**

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☒ Formal Number of Sheets 2
   b. ☐ Informal Number of Sheets _____
4. ☒ Oath or Declaration
   a. ☐ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☒ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c. ☐ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☒ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy *(identical to computer copy)*
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

**Accompanying Application Parts**

8. ☒ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☒ Certificate of Mailing
    ☐ First Class ☒ Express Mail *(Specify Label No.):* EL 394 376 670 US

# UTILITY PATENT APPLICATION TRANSMITTAL
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*(Only for new nonprovisional applications under 37 CFR 1.53(b))*

| Docket No. |
|---|
| 11675.114.1 |
| Total Pages in this Submission |
| 23 |

**Accompanying Application Parts (Continued)**

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

**Fee Calculation and Transmittal**

**CLAIMS AS FILED**

| For | #Filed | #Allowed | #Extra | | Rate | Fee |
|---|---|---|---|---|---|---|
| **Total Claims** | 20 | - 20 = | 0 | x | $18.00 | $0.00 |
| **Indep. Claims** | 6 | - 3 = | 3 | x | $78.00 | $234.00 |
| **Multiple Dependent Claims (check if applicable)** ☐ | | | | | | $0.00 |
| | | | | | **BASIC FEE** | $690.00 |
| **OTHER FEE** *(specify purpose)* | | | | | | $0.00 |
| | | | | | **TOTAL FILING FEE** | $924.00 |

☒ A check in the amount of **$924.00** to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **23-3178** as described below. A duplicate copy of this sheet is enclosed.

- ☐ Charge the amount of as filing fee.
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- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

*Signature*

**Bradley K. DeSandro, Reg. No. 34,521**

Dated: **May 25, 2000**

022901

PATENT TRADEMARK OFFICE

cc:

| TRANSMITTAL LETTER<br>(General - Patent Pending) | Docket No.<br>11675.114.1 |
|---|---|

In Re Application Of: **Kei-Yu Ko**

| Serial No. | Filing Date | Examiner | Group Art Unit |
|---|---|---|---|
| **Not yet assigned** | **Herewith** | **Not yet assigned** | **Not yet assigned** |

Title: **GATE STACK STRUCTURE**

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Transmitted herewith is:

**Utility Patent Application Transmittal (3 pgs); Divisional Application (23 pgs); Declaration and Oath; Assignment; Two (2) Sheets of Formal Drawings; Check No. 115702 in the amount of $924.00; Certificate of Mailing by Express Mail, No. EL 394 376 670 US; Postcard**

in the above identified application.

- ☐ No additional fee is required.
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- ☒ The Assistant Commissioner is hereby authorized to charge and credit Deposit Account No. **23-3178** as described below. A duplicate copy of this sheet is enclosed.
  - ☐ Charge the amount of
  - ☒ Credit any overpayment.
  - ☒ Charge any additional fee required.

*Signature*

Dated: **May 25, 2000**

**Bradley K. DeSandro, Reg. No. 34,521**

**022901**

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I certify that this document and fee is being deposited on with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

***Signature of Person Mailing Correspondence***

***Typed or Printed Name of Person Mailing Correspondence***

cc:

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APPLICATION INFORMATION

Title Line One:: GATE STACK STRUCTURE
Total Drawing Sheets:: 2
Formal Drawings?:: Yes
Application Type:: Utility
Docket Number:: 11675.114.1
Secrecy Order in Parent Appl.?:: No

REPRESENTATIVE INFORMATION

Representative Customer Number:: 22901
Registration Number One:: 34521

CONTINUITY INFORMATION

This application is a:: DIVISION OF
> Application One:: 08/846,671
Filing Date:: 04-20-1997

Source:: PrintEFS Version 1.0.1

Express Mailing Label No. EL 394 376 670 US

PATENT APPLICATION
Docket No. 11675.114.1

# UNITED STATES PATENT APPLICATION

of

**Kei-Yu Ko**

for

# GATE STACK STRUCTURE

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This is a divisional application of US Patent Application Serial No. 08/846,671, filed on April 20, 1997, titled "UNDOPED SILICON DIOXIDE AS ETCH STOP FOR SELECTIVE ETCH OF DOPED SILICON DIOXIDE", which is incorporated herein by reference.

## BACKGROUND OF THE INVENTION

### 1. The Field of the Invention

The present invention involves an etching process that utilizes an undoped silicon dioxide layer as an etch stop during a selective etch of a doped silicon dioxide layer that is situated on a semiconductor substrate. More particularly, the present invention relates to a process for selectively utilizing a fluorinated chemistry in a plasma etch system for etching a doped silicon dioxide layer situated upon an undoped silicon dioxide layer that acts as an etch stop.

### 2. The Relevant Technology

Modern integrated circuits are manufactured by an elaborate process in which a large number of electronic semiconductor devices are integrally formed on a semiconductor substrate. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including but not limited to bulk semiconductive material such as a semiconductive wafer, either alone or in assemblies comprising other materials thereon, and semiconductive material layers, either alone or in assemblies comprising other materials. The term substrate refers to any supporting structure including but not limited to the semiconductive substrates described above.

Conventional semiconductor devices which are formed on a semiconductor substrate include capacitors, resistors, transistors, diodes, and the like. In advance manufacturing of integrated circuits, hundreds of thousands of these semiconductor devices are formed on a single semiconductor substrate. In order to compactly form the semiconductor devices, the

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semiconductor devices are formed on varying levels of the semiconductor substrate. This requires forming a semiconductor substrate with a topographical design.

The semiconductor industry is attempting to increase the speed at which integrated circuits operate, to increase the density of devices on the integrated circuits, and to reduce the price of the integrated circuits. To accomplish this task, the semiconductor devices used to form the integrated circuits are continually being increased in number and decreased in dimension in a process known as miniaturization.

One component of the integrated circuit that is becoming highly miniaturized is the active region. An active region is a doped area in a semiconductor substrate that is used together with other active regions to form a diode or a transistor. The miniaturization of the active region complicates the formation of the interconnect structure in that, in order to maintain sufficient electrical communication, the interconnect structure must be formed in exact alignment with the active region. Also, the area of the interconnect structure interfacing with the active region must be maximized. Thus, less area is provided as tolerance for misalignment of the interconnect structure.

The increasing demands placed upon manufacturing requirements for the interconnect structure have not been adequately met by the existing conventional technology. For example, it is difficult at greater miniaturization levels to exactly align the contact hole with the active region when patterning and etching the contact hole. As a result, topographical structures near the bottom of the contact hole upon the active region can be penetrated and damaged during etching of the contact hole. The damage reduces the performance of the active region and alters the geometry thereof, causing a loss of function of the semiconductor device being formed and possibly a defect condition in the entire integrated circuit. To remedy these problems, the prior art uses an etch stop to prevent over etching.

In a conventional self-aligned etch process for a contact hole, a silicon nitride layer or cap is usually used on top of a gate stack as an etch stop layer during the self-aligned

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contact etch process. One of the problems in the prior art with forming a silicon nitride cap was the simultaneous formation of a silicon nitride layer on the back side of the semiconductor wafer. The particular problems depend on the process flow. For instance, where a low pressure chemical vapor deposition is used to deposit silicon nitride, both sides of the semiconductor wafer would receive deposits of silicon nitride. The presence of the silicon nitride on the back side of the semiconductor wafer causes stress which deforms the shape of the semiconductor wafer, and can also potentially cause deformation of the crystal structure as well as cause defects in the circuit. Additionally, silicon nitride deposition is inherently a dirty operation having particulate matter in abundance which tends to reduce yield. When a low pressure chemical vapor deposition process is utilized, the silicon nitride layering on the back side of the semiconductor wafer must be removed later in the process flow.

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## SUMMARY OF THE INVENTION

The present invention relates to a process for selectively plasma etching a semiconductor substrate to form a designated topographical structure thereon utilizing an undoped silicon dioxide layer as an etch stop. In one embodiment, a substantially undoped silicon dioxide layer is formed upon a layer of semiconductor material. A doped silicon dioxide layer is then formed upon the undoped silicon dioxide layer. The doped silicon dioxide layer is etched to create a topographical structure. The etch has a material removal rate that is at least 10 times higher for doped silicon dioxide than for the undoped silicon dioxide or the layer of semiconductor material.

One application of the inventive process includes a multilayer structure situated on a semiconductor substrate that comprises layers of a semiconductor material, a thin silicon dioxide layer, a layer of conductor material, and a refractory metal silicide layer. By way of example, the multilayer structure situated on a semiconductor substrate may consist of a gate oxide situated on a silicon substrate, a layer of polysilicon, and a refractory metal silicide layer on the layer of polysilicon. A substantially undoped silicon dioxide layer is then formed over the multilayer structure.

The multilayer structure is then patterned to form the designated topography. Doped silicon dioxide is then formed on the semiconductor substrate as a passivation layer. A photoresist layer is utilized to expose selected portions of the doped silicon dioxide layer that are intended to be etched. One example of a topographical structure created utilizing this process are gate stacks. The doped silicon dioxide is then selectively and anisotropically etched with a carbon fluorine etch recipe so as to self-align contact holes down to the semiconductor substrate between the gate stacks.

Each gate stack has a cap composed of substantially undoped silicon dioxide. A layer of silicon nitride or undoped silicon dioxide is deposited over the gate stacks and the semiconductor substrate therebetween. A spacer etch is performed to create silicon nitride

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or undoped silicon dioxide spacers on the side of each gate stack. The silicon nitride or undoped silicon dioxide spacers are generally perpendicular to the base silicon layer.

The present invention contemplates a plasma etching process for anisotropic etching a doped silicon dioxide layer situated on an undoped silicon dioxide layer that acts as an etch stop. One application of the present invention is the formation of gate stacks having spacers composed of substantially undoped silicon dioxide. The undoped silicon dioxide spacers act as an etch stop. Novel gate structures are also contemplated that use a substantially undoped silicon dioxide etch stop layer for a carbon fluorine etch of a doped silicon dioxide layer, where the substantially undoped silicon dioxide etch stop layer resists etching by a carbon fluorine etch.

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## BRIEF DESCRIPTION OF THE DRAWINGS

In order that the manner in which the above-recited and other advantages and objects of the invention are obtained, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are therefore not to be considered limiting of its scope, the invention will be described with additional specificity and detail through the use of the accompanying drawings in which:

Figure 1 is a partial cross-sectional elevation view of one embodiment of a multilayer structure prior to an etch, the multi-layer structure including a base silicon layer and a layer of undoped silicon dioxide, where the multi-layer structure has a layer of photoresist, and wherein a first selected pattern is defined in phantom.

Figure 2 is a partial cross-sectional elevation view of the structure seen in Figure 1, wherein the layer of undoped silicon dioxide has been etched so as to form a recess terminating upon the base silicon layer, a layer of doped silicon dioxide has been deposited thereover, where a layer of photoresist is formed over the layer of doped silicon dioxide, and wherein a second selected pattern is defined in phantom which is intended to represent an etch through the layer of doped silicon dioxide to expose a contact on the base silicon layer that is self-aligned between the layer of undoped silicon dioxide, wherein the self-alignment of the etch is due to the selectivity of the etch to undoped silicon dioxide.

Figure 3 is a partial cross-sectional elevation view of one embodiment of a multilayer structure prior to an etch, the multilayer structure including a base silicon layer and having thereon layers of gate oxide, polysilicon, tungsten silicide, and undoped silicon dioxide, where the multi-layer structure has a layer of photoresist, and wherein a first selected pattern is defined in phantom.

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Figure 4 is a partial cross-sectional elevation view of the structure seen in Figure 3, wherein gate stacks are formed upon the base silicon layer, each gate stack having a spacer on a sidewall thereof and a cap on the top thereof, the gate stacks having deposited thereover a layer of doped silicon dioxide, and a layer of photoresist is deposited upon the layer of doped silicon dioxide, wherein a second selected pattern is defined in phantom which is intended to represent a fluorinated chemical etch through the layer of doped silicon dioxide to expose a contact on the base silicon layer that is self-aligned between the gate stacks, wherein the self-alignment of the etch is due to the selectivity of the etch to the materials of the spacers and the cap of the gate stacks.

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## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The inventive process herein is directed towards selectively utilizing a plasma etch system on doped silicon dioxide ($SiO_2$) layer with a substantially undoped silicon dioxide layer as an etch stop. One application of the inventive process is to form a self-aligned contact. The present invention also discloses an inventive multilayer gate structure.

As illustrated in Figure 1, one embodiment of a multilayer structure 10 is created that comprises a base silicon layer 12. Overlying silicon base layer 12 is a substantially undoped silicon dioxide layer 22. Undoped silicon dioxide layer 22 can be any type of undoped oxide and be formed by a thermal process, by a plasma enhanced deposition process, or by a conventional TEOS precursor deposition that is preferably rich in carbon or hydrogen, or by a precursor of gaseous silane ($SiH_4$) with oxygen. In the latter process, the gaseous silane flow will result in undoped silicon dioxide layer 22.

The next layer in the embodiment of multilayer structure 10 illustrated in Figure 1 comprises a photoresist layer 24 that is processed to expose a first selected pattern 15, shown in phantom, such that silicon dioxide layer 22 will be used to create a topography in multilayer structure 10. Multilayer structure 10 is then anisotropically etched as shown by first selected pattern 15 to selectively remove material from undoped silicon dioxide layer 22 to form undoped silicon dioxide caps 16 as seen in Figure 2.

A doped silicon dioxide layer 30 is deposited over multilayer structure 10 as a passivation layer. Preferably, doped silicon dioxide layer 30 is substantially composed of borophosphosilicate glass (BPSG), borosilicate glass (BSG), or phosphosilicate glass (PSG). Most preferably, doped silicon dioxide layer 30 is substantially composed of silicon dioxide having doping of about 3% or more for boron and about 3% or more for phosphorus. A photoresist layer 32 is applied over doped silicon dioxide layer 30. Photoresist layer 32 is processed to expose a second selected portion 17 of doped silicon dioxide layer 30 that is intended to be etched. Second selected portion 17 is seen in phantom in Figure 2.

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The structure seen in Figure 2 is now etched with a fluorinated or fluoro-carbon chemical etchant system to form second selected pattern 17 as illustrated in Figure 2. The preferred manner is an anisotropic plasma etch of doped silicon dioxide layer 30 down to the corresponding etch stop layer of undoped silicon dioxide cap 16. The plasma etch technique employed herein is preferably generated under a vacuum within the confines of a discharging unit and involves any type of a plasma system, including a high density plasma etcher. A conventional radio frequency reactive ion etcher (RF RIE) plasma system, a magnetically enhanced RIE (MERIE) plasma system, or an inductively coupled plasma system could be used. The preferred embodiment, however, is an RF type RIE or MERIE plasma system. It is preferred the plasma system being used has a plasma density in a range from about $10^9$ /cm$^3$ to about $10^{11}$ /cm$^3$ A high density plasma system can also be used having a plasma density in a range from about $10^{12}$ /cm$^3$ to about $10^{13}$ /cm$^3$

One particular embodiment of a specific structure created utilizing the inventive process is illustrated in Figure 3 wherein a multilayer structure 50 is created that comprises a base silicon layer 12. Overlying silicon base layer 12 is a gate oxide layer 14 that covers silicon base layer 12. Gate oxide layer 14 may be relatively thin in comparison with the other layers of the multilayered structure. The next layer in multilayer structure 50 comprises a polysilicon gate layer 18. Overlying polysilicon gate layer 18 is a refractory metal silicide layer 20. A known benefit of refractory metal silicides is their low resistivity. Refractory metal silicide layer 20 may comprise any refractory metal including but not limited to titanium, tungsten, tantalum, and molybdenum. Preferably, refractory metal silicide layer 20 is substantially composed of tungsten silicide ($WSi_x$).

Overlying refractory metal silicide layer 20 is a substantially undoped silicon dioxide layer 22 which can be formed thermally, by plasma enhanced deposition, by a conventional TEOS precursor deposition that is preferably rich in carbon or hydrogen, or by a precursor of gaseous silane ($SiH_4$) with oxygen. The next layer in multilayer structure 50 is a

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photoresist layer 24 that is processed to expose a first selected pattern 15 shown in phantom. Multilayer structure 50 is then etched according to first selected pattern 15 to selectively remove material so as to form gate stacks 26 as illustrated in Figure 4. Each gate stack 26 has an undoped silicon dioxide cap 52 thereon which was formed from undoped silicon dioxide layer 22.

A spacer 28 in on the sidewall of each gate stack 26. Spacers 28 are formed by subjecting a layer of silicon nitride deposited over gate stacks 26 to a spacer etch. Silicon nitride spacers 28 are generally perpendicular to silicon base layer 12. Alternatively, spacers 28 can be substantially composed of undoped silicon dioxide. As such, both spacers 28 and undoped silicon dioxide caps 52 can be made from the same materials and both act as an etch stop.

Once gate stacks 26 are formed, a contact 34 is defined therebetween upon silicon base layer 12. At this point in the processing, a doped silicon dioxide layer 30, composed of a material such as PSG, BSG, or BPSG, is deposited over multilayer structure 50. A photoresist layer 32 is then applied over doped silicon dioxide layer 30. Photoresist layer 32 is processed to create a second selected pattern 17 that is illustrated in phantom in Figure 4.

The structure seen in Figure 4 is now etched with a fluorinated or fluoro-carbon chemical etchant system according to second selected pattern 17. The preferred manner of etching of doped silicon dioxide layer 30 down to its corresponding etch stop layer, which is substantially undoped silicon dioxide layer 52, is by a plasma etch. The etch technique employed herein is preferably a plasma etch involving any type of a plasma system including a high density plasma etcher as previously discussed relative to Figure 2.

One factor that effects the etch rate and the etch selectivity of the process is pressure. The total pressure has a preferred range from about 1 millitorr to about 400 millitorr. A more preferred pressure range for a plasma etch is in a pressure range from about 1 millitorr to about 100 millitorr. The most preferred pressure range for a plasma etch is from about

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1 millitorr to about 75 millitorr. The pressure may be increased, however, above the most preferred ranges. For example, the RIE etch may be performed at about 100 millitorr. Selectivity can be optimized at a pressure range between about 10 millitorr and about 75 millitorr. Pressure increases may result in a loss in selectivity. The range in selectivity, however, can be adjusted to accommodate different pressures. As such, selectivity and pressure are inversely related.

Temperature is another factor that effects the selectivity of the etching process used. A preferable temperature range during the plasma etch has a range of about 10°C to about 80°C, and more preferably about 20°C to about 40°C. This is the temperature of a bottom electrode adjacent to silicon layer 12 during the etching process. The preferable range of the semiconductor materials is between about 40°C and about 130°C, and more preferably between about 40°C and about 90°C.

Undoped silicon dioxide cap 52 and silicon nitride spacers 28 protect gate stacks 26 from the fluorinated chemical etch. As illustrated in Figure 4, the etch will selectively and anisotropically remove doped silicon dioxide layer 30 above contact 34 as indicated by second selected pattern 17. The etch removes material from doped silicon dioxide layer 30 at a higher material removal rate than that of undoped silicon dioxide cap 52 and silicon nitride spacers or undoped silicon dioxide spacers 28. Preferably, the etch has a material removal rate for doped silicon dioxide is at least 10 times higher than that of undoped silicon dioxide. As such contact 34 is self-aligned between spacers 28 of gate stacks 26. The self-aligning aspect of contact 34 is due to the selectivity of the etch which assures that even in cases of misalignment of the exposure of second selected pattern 17, the fluorinated chemical etch through doped silicon dioxide layer 30 will properly place contact 34 on silicon base layer 12 and between adjacent silicon nitride spacers 28 that have been formed upon sides of gate stacks 26.

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Contact 34 is preferably exposed by an anisotropic plasma etch with a fluorinated chemistry that etches through BSG, PSG, BPSG, or doped silicon dioxide in general. The etch is preferably selective to undoped silicon dioxide, silicon, and silicon nitride. The fluorinated chemical etch utilizes a type of carbon fluorine gas from the group consisting of $C_2F_6$, $CF_4$, $C_3F_8$, $C_4F_{10}$, $C_2F_8$, $CH_2F_2$, $CHF_3$, $C_2HF_5$, $CH_3F$ and combinations thereof. There are other fluorinated enchants in a substantially gas phase during the etching of the structure. An inert gas is often used in combination with the fluorinated etchant. Argon, nitrogen, and helium are examples of such an inert gas. The preferred gasses, however, are $CF_4$, $CH_2F_2$, $CHF_3$ and Ar. Alternatively $CH_3F$ may be used in place of $CH_2F_2$. In particular, the preferred enchant is a fluorine deficient gas which is defined as a gas where there are not enough fluorine atoms to saturate the bonding for the carbon atoms.

A conductive material is formed upon contact 34 between spacers 28 within second selected pattern 17 as shown in Figure 4. The conductive material will form a contact plug to contact 34. It may be desirable to clad the contact plug with a refractory metal or a refractory metal silicide. As such, second selected pattern 17 would have proximate thereto the refractory metal or silicide thereof prior to formation of the contact plug in contact with contact 34.

The present invention has application to a wide variety of structures. The top layer of the gate stack, composed of undoped silicon dioxide, can be used to create and protect various types of structures during the doped silicon dioxide etching process for structures other than gate stacks.

The present invention allows the gate stack height to be reduced. One advantage of reducing the gate stack height is to reduce the process time which results in greater throughput. The reduced gate height results in a lower etch time and a reduced contact hole aspect ratio, the latter being defined as the ratio of height to width of the contact hole. By reducing the aspect ratio, or by reducing the height of the gate stack, there will be a decrease

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in the etch time. Another advantage of a lower gate stack height is that it reduces the overall topography which in turn results in it being easier to planarize and to use photolithographic processes. As such, the present invention increases yield.

The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

What is claimed and desired to be secured is:

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1. A gate stack structure situated over a base semiconductor material layer, said gate stack structure comprising:

a gate oxide layer on said base semiconductor material layer;

a gate layer, composed of a first conductive material, on said gate oxide layer;

a layer of refractory metal silicide on said gate layer;

an undoped silicon dioxide cap on said layer of refractory metal silicide;

a spacer over a lateral side of the gate layer and in contact with said base semiconductor material layer, said spacer being composed of a nonconductive material, wherein the lateral side of the gate layer is oriented perpendicular to said base semiconductor material layer;

a contact plug in contact with said base semiconductor material layer composed of a second conductive material, and being situated adjacent to the gate layer; and

a layer of doped silicon dioxide over said spacer, over said undoped silicon dioxide cap, and in contact with said contact plug.

2. The gate stack structure as recited in Claim 1, wherein said nonconductive material is composed of silicon nitride.

3. The gate stack structure as recited in Claim 1, wherein:

said nonconductive material is composed of undoped silicon dioxide; and

the spacer is integral with the undoped silicon dioxide cap.

4. The gate stack structure as recited in Claim 1, wherein the semiconductor material is monocrystalline silicon.

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5. The gate stack structure as recited in Claim 1, wherein said refractory metal silicide layer is tungsten silicide.

6. The gate stack structure as recited in Claim 1, wherein said layer of doped silicon dioxide layer is composed of a material selected from the group consisting of BPSG, PSG, and BSG.

7. The gate stack structure as recited in Claim 1, wherein the spacer is composed of a material that is one of silicon nitride and undoped silicon dioxide.

8. The gate stack structure as defined in Claim 1, wherein the first conductive material is polysilicon.

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9. A gate stack structure situated over a base monocrystalline silicon layer, said gate stack structure comprising:

a gate oxide layer on said base monocrystalline silicon layer;

a polysilicon gate layer on said gate oxide layer;

a layer of tungsten silicide on said polysilicon gate layer;

an undoped silicon dioxide cap on said layer of tungsten silicide;

a spacer over a lateral side of the gate layer and in contact with said base monocrystalline silicon layer, said spacer being composed of undoped silicon dioxide and being integral with the undoped silicon dioxide cap, wherein the lateral side of the gate layer is oriented perpendicular to said base monocrystalline silicon layer;

a contact plug in contact with said base monocrystalline silicon layer and being:

composed of a second conductive material; and

situated adjacent to the gate layer; and

a layer of doped silicon dioxide being composed of a material selected from the group consisting of BPSG, PSG, and BSG, and being situated over said spacer, over said undoped silicon dioxide cap, and in contact with said contact plug.

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10. A gate stack structure situated over a base monocrystalline silicon layer, said gate stack structure comprising:

a gate oxide layer on said base monocrystalline silicon layer;

a polysilicon gate layer on said gate oxide layer;

a layer of tungsten silicide on said polysilicon gate layer;

an undoped silicon dioxide cap on said layer of tungsten silicide;

a spacer over a lateral side of the gate layer and in contact with said base monocrystalline silicon layer, said spacer being composed of of a material that is one of silicon nitride and undoped silicon dioxide and being integral with the undoped silicon dioxide cap, wherein the lateral side of the gate layer is oriented perpendicular to said base monocrystalline silicon layer;

a contact plug in contact with said base monocrystalline silicon layer and being:

composed of a second conductive material; and

situated adjacent to the gate layer; and

a layer of doped silicon dioxide being composed of a material selected from the group consisting of BPSG, PSG, and BSG, and being situated over said spacer, over said undoped silicon dioxide cap, and in contact with said contact plug.

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11. A gate structure comprising:

a pair of gate stacks situated over a base semiconductor material layer, each said gate stack comprising:

a gate oxide layer on said base semiconductor material layer;

a gate layer, composed of a first conductive material, on said gate oxide layer;

a layer of refractory metal silicide on said gate layer;

an undoped silicon dioxide cap on said layer of refractory metal silicide; and

a spacer in contact with a lateral side of each said gate stack and with said base semiconductor material layer, said spacer being composed of a nonconductive material, each said lateral side of each said gate stack being perpendicular to said base semiconductor material layer;

a contact plug in contact with said base semiconductor material layer composed of a second conductive material, and being situated between said pair of gate stacks; and

a layer of doped silicon dioxide over said spacer, over said undoped silicon dioxide cap, and in contact with said contact plug.

12. A gate structure as recited in Claim 11, wherein said nonconductive material is composed of silicon nitride.

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13. The gate structure as recited in Claim 11, wherein:

said nonconductive material is composed of undoped silicon dioxide; and

each said spacer is integral with a respective one of said undoped silicon dioxide caps.

14. A process as recited in Claim 11, wherein the semiconductor material is monocrystalline silicon.

15. A process as recited in Claim 11, wherein said refractory metal silicide layer is tungsten silicide.

16. A process as recited in Claim 11, wherein said layer of doped silicon dioxide layer is composed of a material selected from the group consisting of BPSG, PSG, and BSG.

17. A process as recited in Claim 11, wherein the spacer is composed of a material that is one of silicon nitride and undoped silicon dioxide.

18. A gate structure as defined in Claim 11, wherein the first conductive material is polysilicon.

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19. A gate structure comprising:

a pair of gate stacks situated over a base monocrystalline silicon layer, each said gate stack comprising:

a gate oxide layer on said base monocrystalline silicon layer;

a polysilicon gate layer on said gate oxide layer;

a layer of tungsten silicide on said polysilicon gate layer;

an undoped silicon dioxide cap on said layer of tungsten silicide; and

a spacer over a lateral side of each said gate stack and in contact with said base monocrystalline silicon layer, said spacer being composed of undoped silicon dioxide and being integral with the undoped silicon dioxide cap, wherein the lateral side of each said gate stack is oriented perpendicular to said base monocrystalline silicon layer;

a contact plug in contact with said base monocrystalline silicon layer and being composed of a second conductive material, and being situated between said pair of gate stacks; and

a layer of doped silicon dioxide over said spacer, over said undoped silicon dioxide cap, and in contact with said contact plug.

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20. A gate structure comprising:

a pair of gate stacks situated over a base monocrystalline silicon layer, each said gate stack comprising:

a gate oxide layer on said base monocrystalline silicon layer;

a polysilicon gate layer on said gate oxide layer;

a layer of tungsten silicide on said polysilicon gate layer;

an undoped silicon dioxide cap on said layer of tungsten silicide; and

a spacer over a lateral side of each said gate stack and in contact with said base monocrystalline silicon layer, said spacer being composed of a material that is one of silicon nitride and undoped silicon dioxide, each said lateral side of each said gate stack being perpendicular to said base monocrystalline silicon layer;

a contact plug in contact with said base monocrystalline silicon layer and being composed of a second conductive material, and being situated between said pair of gate stacks; and

a layer of doped silicon dioxide over said spacer, over said undoped silicon dioxide cap, and in contact with said contact plug.

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## ABSTRACT OF THE INVENTION

The present invention relates to gate stack structure that is fabricated by a process for selectively plasma etching a structure upon a semiconductor substrate to form a designated topographical structure thereon utilizing an undoped silicon dioxide layer as an etch stop. In one embodiment, a substantially undoped silicon dioxide layer is formed upon a layer of semiconductor material. A doped silicon dioxide layer is then formed upon said undoped silicon dioxide layer. The doped silicon dioxide layer is etched to create the topographical structure. The etch has a material removal rate that is at least 10 times higher for doped silicon dioxide than for undoped silicon dioxide or the semiconductor material. One application of the inventive process includes selectively plasma etching a multilayer structure to form a self-aligned contact between adjacent gate stacks and a novel gate structure resulting therefrom. In the application, a multilayer structure is first formed comprising layers of silicon, gate oxide, polysilicon, and tungsten silicide. An undoped silicon dioxide layer is formed over the multilayer structure. After patterning and etching, the multilayer structure to form gate stacks therefrom, a layer silicon nitride is deposited and is etched to create spacers on the gate stacks that are generally perpendicular to the silicon layer. Doped silicon dioxide is then deposited over the gate stacks and corresponding spacers. A photoresist layer is utilized to expose selective portions of silicon dioxide layer above the contacts on the silicon layer that are to be exposed by etching down through the doped silicon dioxide layer. The doped silicon dioxide is then selectively etched using an anisotropical plasma etch that utilizes a carbon fluorine etch. The novel gate stack structure comprising an undoped silicon dioxide cap is capable of resisting a carbon fluorine etch.

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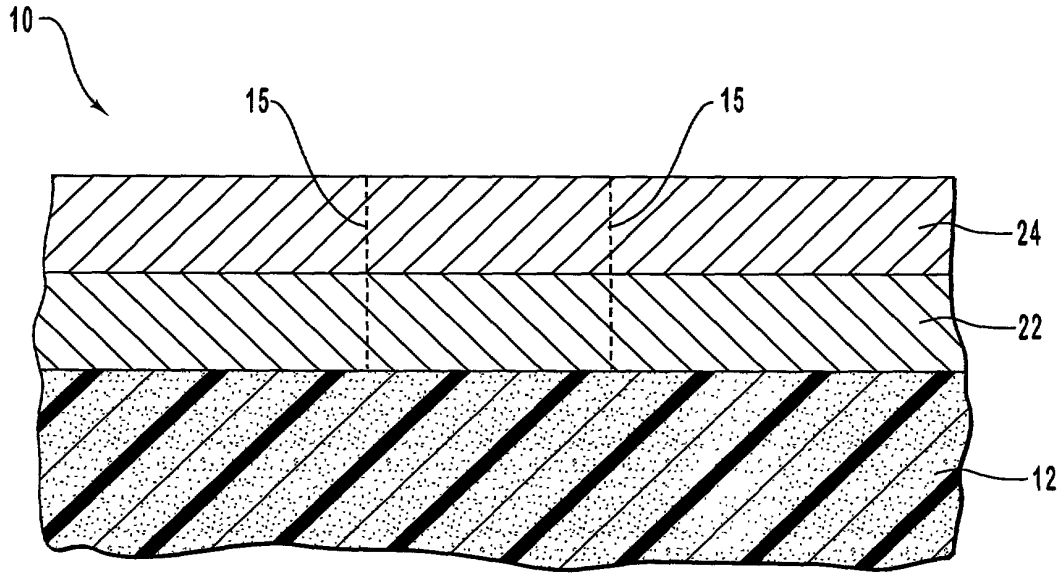


FIG. 1

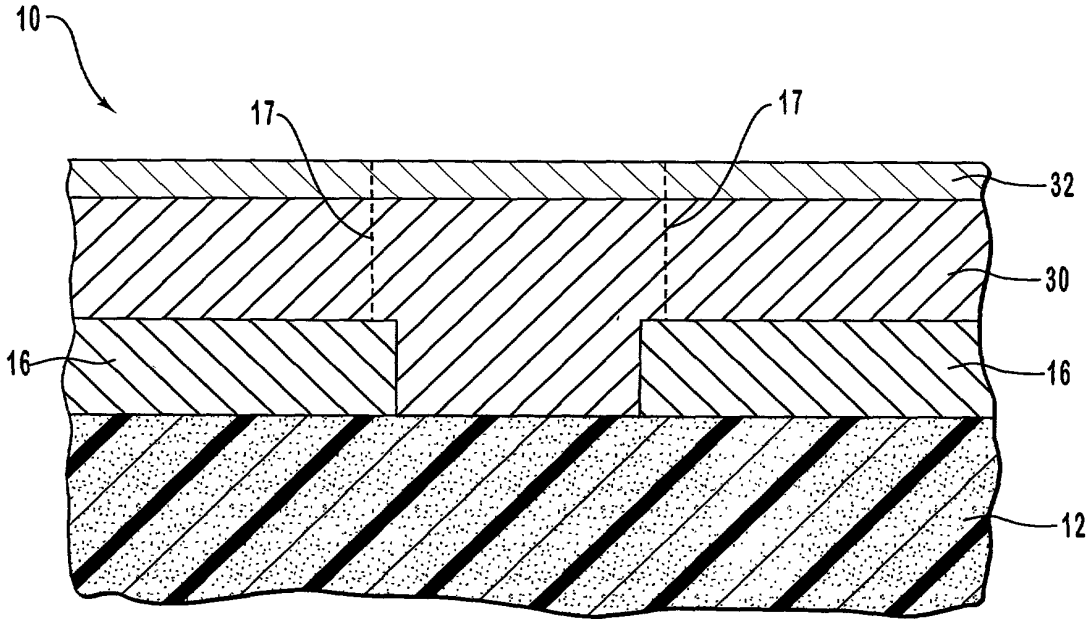


FIG. 2

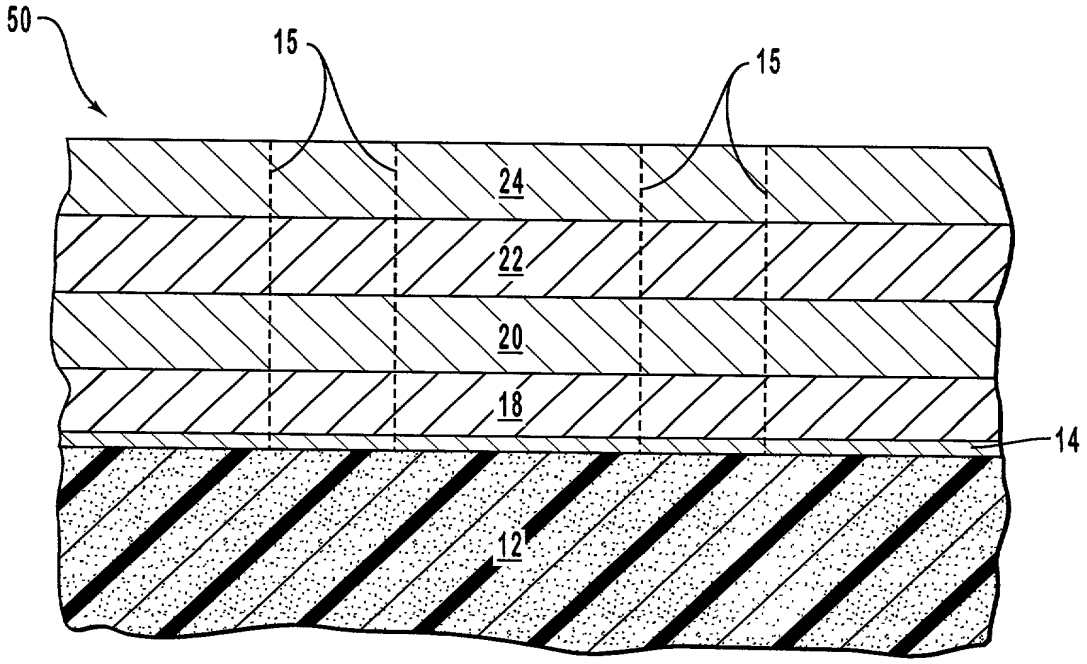
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FIG. 3

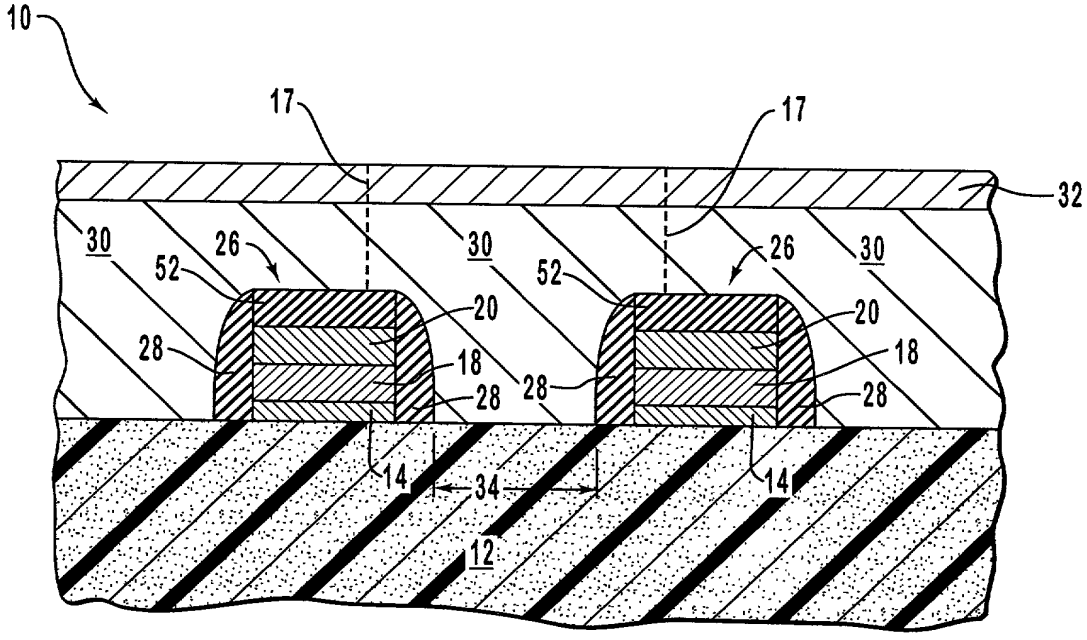
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FIG. 4

PATENT APPLICATION
Docket No: 11675.114

DECLARATION, POWER OF ATTORNEY, AND PETITION

I, Kei-Yu Ko, declare: that I am a citizen of the United States of America; that my residence and post office address is 4611 E. Rockbury Ct., Meridian, Idaho 83642; that I verily believe I am the original, first, and sole inventor of the subject matter of the invention or discovery entitled UNDOPED SILICON DIOXIDE AS ETCH STOP FOR SELECTIVE ETCH OF DOPED SILICON DIOXIDE, for which a patent is sought and which is described and claimed in the specification attached hereto; that I have reviewed and understand the contents of the above-identified specification, including the claims; and that I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Section 1.56(a) of Title 37 of the Code of Federal Regulations.

I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

I hereby appoint as my attorneys and/or patent agents: H. ROSS WORKMAN, Registration No. 25,230; RICK D. NYDEGGER, Registration No. 28,651; DAVID O. SEELEY, Registration No. 30,148; JONATHAN W. RICHARDS, Registration No. 29,843; JOHN C. STRINGHAM, Registration No. P-40,831; MICHAEL F. KRIEGER, Registration No. 35,232; BRADLEY K. DeSANDRO, Registration No. 34,521; JOHN M. GUYNN, Registration No. 36,153; GREGORY

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BRADLEY K. DeSANDRO
WORKMAN, NYDEGGER & SEELEY
1000 Eagle Gate Tower
60 East South Temple
Salt Lake City, Utah 84111

Wherefore, I pray that Letters Patent be granted to me for the invention or discovery described and claimed in the foregoing specification and claims, declaration, power of attorney, and this petition.

Signed at Boise, Idaho, this 28 day of April, 1997

Inventor: _____
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4611 E.Rockbury Ct.
Meridian, Idaho 83642

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